IN THE CLAIMS

Please cancel claims 1-5 and 15-17

Please amend claims 6, 11 and 12 as follows:

1.-5. (Cancelled)

6. (Currently amended) A semiconductor chip with a top side, a rear side, and with edge sides, the semiconductor chip comprising:

an integrated circuit on the top side;

at least one edge side having edge contacts wherein, the edge contacts extend from the top side in the direction of the rear side of the semiconductor chip; and

wherein the edge contacts are connected to electrodes of the integrated circuit via conductor tracks located on the top surface of the semiconductor chip.

wherein a plurality of additional semiconductor chips are ~~stacked one on the other and are~~ electrically connected via the edge contacts among one another and also with respect to external contacts on ~~an insulated~~ a circuit substrate such that the rear sides of the semiconductor ~~wafers~~ chips are oriented virtually perpendicular to a top side of the circuit substrate.

7. (Previously Presented) The semiconductor chip of claim 6, wherein the edge sides have a perforation-like structure, semicylinder-like cutouts extending as edge contacts from the top side in the direction of the rear side, and have a metal layer.

8. (Original) The semiconductor chip of claim 7, wherein the edge sides also have an insulation layer.

9. (Original) The semiconductor chip of claim 7, wherein the cutouts have a soldering material.

10. (Original) The semiconductor chip of claim 7, wherein the edge contacts are extended on the top side to form a contact area and merge with a conductor track on the top side.

11. (Currently amended) The semiconductor chip of claim 7 arranged on [[a]] the circuit substrate within an electronic component.

12. (Currently amended) The semiconductor chip of claim 11, wherein the top side of the circuit substrate has a ~~top side and a~~ conductor track structure, the semiconductor chip being arranged with its rear side on the top side of the circuit substrate and the edge contacts being electrically connected to the conductor track structure via contact pads on the top side of the circuit substrate.

13. (Previously Presented) The semiconductor chip of claim 12, wherein an insulating plastics composition is arranged on the circuit substrate in a manner embedding the edge sides of the semiconductor chip and the contact pads.

14. (Original) The semiconductor chip of claim 12, wherein the semiconductor chip is arranged with an edge side on the circuit substrate, the top side of the semiconductor chip being arranged in angular fashion with respect to the top side of the circuit substrate and the edge contacts being electrically connected to the contact pads.

15.-17. (Cancelled)

18. (Previously presented) A semiconductor assembly comprising:

a plurality of electronic semiconductor memory chips; and

an insulating circuit substrate comprising lines running parallel on its top side providing a bus line;

wherein the electronic semiconductor memory chips have edge contacts filled with solder material only in an edge region; and

wherein the rear side of the electronic semiconductor memory chips are oriented virtually perpendicular to the top side of the circuit substrate and said edge region is arranged on the top side of the insulating circuit substrate and up so that the plurality of electronic semiconductor memory chips are connected to parallel via the bus line.

19. (Previously presented) The semiconductor assembly of claim 18, wherein the bus line is an address line and the insulating circuit substrate further comprises control lines which drive individual electronic components.

20. (Previously presented) The semiconductor assembly of claim 18, wherein the edge region provided with edge contacts is electrically protected by a plastics composition and wherein the orientation of the electronic component of semiconductor chip size is supported and fixed by the plastics composition in the edge region on circuit substrate.